REMARKS/ARGUMENTS

Claims 1, 4, 5, 10-15 and 19-22 remain in the application.

Claim 1 is amended.

Elections/Restrictions

Claims 1-22 were subject to a restriction requirement and election of genus and species. Claims 1, 4, 5, 10-15 and 19-22 were elected for prosecution in the present application. Claims 2, 3, 6-9 and 16-18 are hereby cancelled. However, the Applicant reserves the right to pursue the non-elected claims in one or more Divisional applications filed during the pendency of the present application.

Claim Rejections Under 35 USC § 103

Claims 1, 4, 5, 10-15 and 19-22 were rejected under 35 USC § 103(a) over admitted prior art in view of US Patent 6,784,530 to Sugaya.

The invention as originally presented is patentable over both the admitted prior art and Sugaya, individually and in combination.

The admitted prior is limited to conventional MEMS devices having a MEMS sensor or actuator device mechanism that is formed in the interior portion of an epitaxial silicon mechanism layer suspended from a peripheral frame and bonded to an inner surface of a bottom cover plate and covered by a top cover plate. Gold traces electrical conductors are formed on the inner surface of the bottom substrate or cover plate. The electrical conductors are electrically interconnected to the device mechanism and extend outwardly across the inner surface of the bottom cover plate to the metal wire bond pads that are positioned on the bottom cover plate inner surface remote from the device mechanism and which thereby provide remote electrical access to the device mechanism. See, e.g., page 3, line 24 - page 7, line 18.

All signals into and out of the device mechanism must be routed on the device mechanism bottom surface. While communication with the device mechanism bottom surface is accommodated, communication with the device mechanism upper surface must be by electrical paths coupled through the bottom surface. Page 7, lines 19-31.

Communication with the top substrate or cover plate must also be routed through the electrical conductors and wire bond pads on the inner surface of the bottom substrate. Because the top substrate is spaced away from the bottom substrate by the mechanism layer,

communication with top substrate must be routed through the device mechanism or the mechanism layer generally. These signal routing limitations demand very complex designs to accommodate communication with the upper device mechanism and substrate surfaces. As a result, the top half of the device is often unused, and the top substrate is provided only as a protective cover for the device mechanism. Page 8, lines 1-9.

Sugaya, referring to FIGS. 12A and 12B, teaches stacked semiconductor packages, wherein a plurality of glass-epoxy substrates 1002 each have a flexible semiconductor chip 1001 coupled thereon by a sealing resin 1006. A projection electrode 1004 is disposed between the semiconductor chip 1001 and a surface electrode 1005 of the glass-epoxy substrate 1002. The glass-epoxy substrates 1002 are stacked so as to form a stacked memory package 1003. A glass-epoxy substrate 1007 is stacked over the top semiconductor chip 1001 with a recessed space 1010 therebetween. A via 1008 through the cover substrate 1007 couples the surface electrode 1005 of the glass-epoxy substrate 1002 to a wiring line 1009 on the cover substrate 1007. Column 1, line 63-column 2, line 8.

Sugaya also teaches a semiconductor chip is mounted on wiring patterns formed on a release carrier, with wiring patterns led from a surface of the semiconductor chip are connected electrically with the inner vias that are formed in the electrical insulating substrate so as to passing therethrough. This allows the circuit component built-in module to be formed with a reduced thickness, as well as allows a stacked module in which circuit components are provided at a high density to be obtained with high performance and a reduced size. Column 4, lines 34-45.

The present invention recited in claim 1 is a MEMS device with a gold stud bump mechanically and electrically coupled between chip bond pads on inner surface of the top and bottom substrates.

The invention as originally recited in claim 1 is patentable over both the admitted prior art and Sugaya, individually and in combination.

The Office Action admits, and the applicant agrees, the admitted prior art fails to disclose or suggest a metal chip bond pad on inner surface of the top substrate, and a gold stud bump mechanically and electrically coupled between chip bond pads on inner surface of the top and bottom substrates. Furthermore, the admitted prior art fails to disclose or suggest a metal chip bond pad on inner surface of the bottom substrate.

Sugaya fails to provide the deficiencies of the admitted prior art. Sugaya fails to disclose or suggest chip bond pads on inner surface of the top and bottom substrates, as recited in claim 1, and further fails to disclose or suggest a gold stud bump mechanically and electrically coupled between chip bond pads on inner surface of the top and bottom substrates, as also recited in claim 1.

The Office Action contends that Sugaya teaches a metal chip bond pad formed on the inner surface of the top substrate 1002 in a complimentary position opposite the chip bond pad 1005 on the bottom substrate; and a stud bump 1008 coupled between the chip bond pads on the top and bottom surfaces. The Office Action cites Figure 12B.

The Office Action is mistaken on both points.

The Office Action fails to point out <u>any</u> metal chip bond pad formed on the inner surface of the top substrate 1002. This is because Sugaya fails to disclose or suggest <u>any</u> metal chip bond pad formed on the inner surface of the top substrate 1002. Rather, Sugaya <u>only</u> teaches a surface electrode 1005 on the <u>upper surface</u> of the stacked glass-epoxy substrates 1002. See, Figures 12A and 12B, and column 1, line 63-column 2, line 8, discussed above.

Sugaya does <u>not</u> teach any surface electrode 1005 on the <u>lower surface</u> of the stacked glass-epoxy substrates 1002. Again, see Figures 12A and 12B, and column 1, line 63-column 2, line 8.

Furthermore, Sugaya does <u>not</u> disclose or suggest a gold stud bump mechanically and electrically coupled between chip bond pads on inner surface of the top and bottom substrates, as recited in claim 1. Rather, Sugaya <u>only</u> teaches a **<u>via 1008</u>** through the cover substrate 1007 that couples the surface electrode 1005 of the glass-epoxy substrate 1002 to a **<u>wiring line 1009</u>** on the cover substrate 1007. Column 1, line 63-column 2, line 8.

Thus, the Office Action is mistaken in believing that the element 1008 is a "stud bump." Rather, the element 1008 is only a conventional <u>via</u> through the cover substrate 1007. The vias 1008 are only circuit pathways through the substrate 1007. Sugaya actually teaches the "vias" 104 being "made of a cured conductive resin composition." The conductive resin is composed of a mixture of metal particles and thermosetting resin. Column 7, lines 43-48.

In contrast, as is well-known in the art, "stud bumps" are free-standing gold or solder balls attached to the chip bond pad as the first part of a wire bond. See, e.g., Specification at page 12,

line 9-page 13, line 2. Thus, the "conductive resin" "vias" 104 taught by fail to disclose or suggest "stud bumps."

Sugaya fails to disclose or suggest any "stud bumps." Rather, Sugaya only teaches "projection electrodes" 1004 disposed between the semiconductor chip 1001 and surface electrodes 1005 of the glass-epoxy substrate 1002. Then a sealing resin 1006 bonds the semiconductor chip 1001 to the substrate 1002. Thus, Sugaya teaches even less than the admitted prior art of the instant application. Only the Specification of the instant application teaches conventional flip chip assemblies. See, e.g., Specification at page 12, lines 3-8.

Obviously, Sugaya fails to disclose or suggest <u>any</u> chip bond pads on inner surface of the top substrate, as recited in claim 1.

Furthermore, Sugaya fails to disclose or suggest <u>any</u> gold stud bump coupled between chip bond pads on inner surface of the top and bottom substrates, as also recited in claim 1.

Regarding the stud bumps being formed of gold, the Office Action contends that Sugaya teaches the "stud bump 1008" being formed of gold, citing column 7, lines 43-48, reproduced here as follows:

> The inner vias 104 may be made of a cured conductive resin composition. The conductive resin composition preferably is composed of a mixture containing 85 wt % to 92 wt % of metal particles and 8 wt % to 15 wt % of a thermosetting resin. Examples applicable as the metal particles include gold, silver, copper, nickel, and the like that have a high conductivity, and mixtures of the same. Column 7, lines 43-48.

Obviously, Sugaya does <u>not</u> teach "stud bumps" being formed of gold. Sugaya only teaches "vias" 104, and the vias 104 are <u>not</u> formed of gold. Rather, the vias 104 are formed of a mixture of epoxy resin and metal particles. In contrast, as is well-known in the art, "stud bumps" are formed "using a modified standard wire bonding technique. This technique makes a conventional gold ball for wire bonding by melting the end of a gold wire to form a sphere. The gold ball is attached to the chip bond pad as the first part of a wire bond." Obviously, a "mixture" of epoxy resin and metal particles, as taught by Sugaya for "vias" 104, <u>cannot</u> form a "stud bump."

For at least the above reasons, claim 1 is allowable as originally filed and without amendment.

However, claim 1 is amended to be broader in scope by reciting a "metal" stud bump in place of the previously recited "gold" stud bump.

Claims 4 and 5 are allowable at least as depending from allowable claim 1.

Claim 4 as originally filed is further allowable independently of base claim 1 as reciting "an electrical path formed on the inner surface of the top substrate and being electrically coupled to the chip bond pad."

The Office Action contends that Sugaya teaches an electrical path formed on the inner surface of the top substrate 1002 and being electrically coupled to the chip bond pad, citing Figure 12B. However, the Office Action fails to point out <u>any</u> such electrical path coupled to the chip bond pad. Rather, as discussed above, Sugaya fails to disclose <u>any</u> chip bond pad on the <u>inner surface of the top substrate 1002</u>. Sugaya <u>only</u> teaches a surface electrode 1005 on the <u>upper surface</u> of the stacked substrates <u>1002</u>. See, Figures 12A and 12B, and column 1, line 63-column 2, line 8, discussed above.

Therefore, Sugaya <u>cannot</u> disclose or suggest <u>any</u> electrical path formed on the inner surface of the top substrate 1002 and being electrically coupled to the chip bond pad, as recited in claim 4.

For at least the above reasons, claim 4 is further allowable independently of allowable base claim 1.

Claim 5 as originally filed is further allowable independently of base claim 1 as reciting the electrical path formed on the inner surface of the top substrate recited in claim 4 being "further electrically coupled to an upper surface of the device mechanism."

The Office Action contends that Sugaya teaches the electrical path formed on the inner surface of the top substrate 1002 is electrically coupled to the upper surface of the mechanism, citing Figure 12B. However, the Office Action fails to point out <u>any</u> such connection in Figure 12B. Rather, as is clearly shown in Figure 12B, the cover substrate 1007 of Sugaya is stacked over the top semiconductor chip 1001 <u>with a **recessed space** 1010 therebetween</u>. See, Figure 12B, and column 1, line 63-column 2, line 8, discussed above.

Therefore, Sugaya <u>cannot</u> disclose or suggest <u>any</u> electrically coupled to the upper surface of the mechanism, as recited in claim 5.

For at least the above reasons, claim 5 is further allowable independently of allowable base claim 1 and intervening dependent claim 4.

Claims 10 and 19 are both different in scope from allowable claim 1. However, the above arguments and reasons for allowance directed to claim 1 are sufficiently applicable to claims 10 and 19 as to make repetition unnecessary. Thus, for each of the reasons above, claims 10 and 19 as originally filed are believed to be allowable over the cited art.

Furthermore, Sugaya fails to disclose or suggest the "gold" stud bumps recited in claims 10 and 19. Rather, as discussed above, Sugaya only discloses a "conductive resin" that is composed of a mixture of gold metal particles and thermosetting resin. Column 7, lines 43-48. As also discussed herein above, the a "mixture" of epoxy resin and metal particles, as taught by Sugaya for "vias" 104, <u>cannot</u> form a "stud bump." Therefore, Sugaya fails to disclose or suggest a "gold" stud bump, as recited in each of claims 10 and 19.

Thus, for these further reasons, claims 10 and 19 are further allowable over Sugaya.

Claims 11-15 are allowable at least as depending from allowable claim 10.

Claim 11 as originally filed is further allowable independently of base claim 10 as reciting electrical conductors formed on the first and second opposing inner substrate surfaces and being electrically coupled to respective first and second ones of the pair of complementary chip bond pads.

The Office Action contends that Sugaya teaches an electrical path formed on the inner surface of the top substrate 1002 and being electrically coupled to the chip bond pad, citing Figure 12B. However, again, the Office Action fails to point out <u>any</u> such electrical path coupled to the chip bond pad. Rather, as discussed above, Sugaya fails to disclose <u>any</u> chip bond pad on the <u>inner surface of the top substrate 1002</u>. Sugaya <u>only</u> teaches a surface electrode 1005 on the <u>upper surface</u> of the stacked substrates <u>1002</u>. See, Figures 12A and 12B, and column 1, line 63-column 2, line 8, discussed above.

Therefore, Sugaya <u>cannot</u> disclose or suggest <u>any</u> electrical path formed on the inner surface of the top substrate 1002 and being electrically coupled to the chip bond pad, as recited in claim 11.

For at least the above reasons, claim 11 is further allowable independently of allowable base claim 10.

Claim 12 as originally filed is further allowable independently of base claim 10 and intervening claim 11 as reciting "<u>each</u> of the first and second electrical conductors further comprises an electrical contact being electrically coupled to the device mechanism."

The Office Action contends that Sugaya discloses that each of the first and second electrical conductors further comprises an electrical contact 1004 being electrically coupled to the device mechanism, citing Figure 12B. However, Sugaya teaches the projection electrode 1004 only between the semiconductor chip 1001 and the surface electrode 1005 of the substrate 1002.

Furthermore, the Office Action fails to point out any such electrical contact between the bottom surface of the cover substrate 1007 and the top semiconductor chip 1001 in Figure 12B. Rather, as is clearly shown in Figure 12B, the cover substrate 1007 of Sugaya is stacked over the top semiconductor chip 1001 with a **recessed space** 1010 therebetween. See, Figure 12B, and column 1, line 63-column 2, line 8, discussed above.

Therefore, Sugaya cannot disclose or suggest any electrically coupled to the upper surface of the mechanism, as recited in claim 12.

For at least the above reasons, claim 12 is further allowable independently of allowable base claim 10 and intervening dependent claim 11.

Claims 20-22 as originally filed are allowable at least as depending from allowable claim 19.

The claims now being in form for allowance, reconsideration and allowance is respectfully requested.

If the Examiner has questions or wishes to discuss any aspect of the case, the Examiner is encouraged to contact the undersigned at the telephone number given below.

Respectfully submitted,

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